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MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

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10/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,433	KNOWLES, SIMON	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 7/14/2009.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger, U.S. Patent No. 5,737,631, in view of Haynes et al., "Configurable Multiplier Blocks for use within an FPGA", 1998 (herein referred to as Haynes), and further in view of Lodi et al., "A Flexible LUT-Based Carry Chain for FPGAs", 2003 (herein referred to as Lodi).

5. Referring to claim 1, Trimberger has taught a computer processor having control and data processing capabilities comprising:

a) a decode unit for decoding instructions (Trimberger: Figure 2, item 112).

b) a dedicated control processing facility comprising a control execution path having its own control register file (Fig.2, component 103, for instance) and an execution unit (Fig.2, component

100). Note that at least these two components may be combined and called a dedicated control processing facility.

c) a dedicated data processing facility having its own data register file (Fig.2, at least component 130), the data processing facility comprising a first data execution path including fixed operators (Trimberger: Figure 2, item 100) and a second data execution path including at least configurable operators (Trimberger: Figure 2, item 120) and a controller (controllers inherently exist in processors). Looking at Fig.2, the dedicated data processing facility could include at least components 100, 103, 120, and 131, where at least components 100 and 103 form the dedicated control processing facility as described above.

d) wherein said decode unit is operable to detect whether a data processing instruction defines a fixed data processing instruction or a configurable data processing instruction, said decode unit causing the computer processor to supply said data processing instruction to said first data execution path for processing when a fixed data processing instruction is detected and to said second data execution path for processing when a configurable data processing instruction is detected (Trimberger: column 7, lines 45-50).

e) Trimberger has not taught that the dedicated control processing facility also includes a branch unit (despite hinting at existence of a branch unit with disclosure of condition codes (Fig.2)) and a load/store unit. However, the examiner asserts that such units are very well known in the art and are advantageous for providing basic functionality. Branch units are clearly advantageous because they allow for execution of branch instructions. These are at least useful so that loops may be implemented. Loops allow for repeated execution of a block of code without writing the code repetitively within the program. Hence, code size may be decreased. Load and stores, on

the other hand, allow for communication data to/from the register file and memory, thereby expanding the usable memory space. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger such that the dedicated control processing facility includes a branch unit and load/store unit.

f) Trimberger has also not taught said configurable operators pre-configured into a plurality of hardwired operator classes. However, both Haynes and Lodi have taught that FPGAs may be designed to include dedicated circuitry pre-configured into a plurality of hardwired operator classes. That is, Haynes has taught dedicated multiplier blocks, which may be programmably interconnected to create larger multipliers. Similarly, Lodi has taught dedicated carry chains, which may be connected to form adders, for instance. See page 133 and section 3.1. Essentially, instead of a fully reprogrammable FPGA, as taught by Trimberger, Haynes and Lodia have taught programmable devices, such as FPGAs, that would include configurable operators pre-configured into hardwired multiplier and carry chain classes. The examiner asserts that it is well known in the art for FPGAs, such as the Xilinx Virtex, to include dedicated multipliers and carry chains. Such a configuration, with a programmable portion, and a dedicated portion, allows a programmer to achieve balance between programmability and speed for different applications. One of ordinary skill in the art would have recognized that the hardwired operators of Haynes and Lodi could be implemented in the FPGA of Trimberger. Such a modification would allow Trimberger to achieve both programmability and speed in cases where dedicated circuitry is faster than programmable circuitry. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger's gate array to include

configurable operators pre-configured into a plurality of hardwired operator classes, as taught by Haynes and Lodi.

g) Trimberger, as modified, has further taught that said controller is operable to configure the connectivity of said configurable operators in accordance with configuration information provided in an opcode portion of said configurable data processing instruction. See column 3, lines 31-33, and note that Trimberger would still select the connectivity of the operator classes via program instruction opcode.

6. Referring to claim 2, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein the decode unit is capable of decoding a stream of instruction packets from memory, each packet comprising a plurality of instructions (Trimberger: column 7, lines 51-56).

7. Referring to claim 3, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein the decode unit is operable to detect if an instruction packet contains a data processing instruction (Trimberger: column 7, lines 45-50).

8. Referring to claim 4, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein the configurable operators are configurable at the level of multi-bit values (Trimberger: column 9, lines 18-19) (The opcode is a multi-bit value).

9. Referring to claim 5, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 4, wherein the configurable operators are configurable at the level of multi-bit values comprising four or more bits (Trimberger: column 9, lines 18-19) (The opcode is at least 4 bits).

10. Referring to claim 6, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 4, wherein the configurable operators are configurable at the level of words (Trimberger: column 9, lines 24-25) (Immediate values are optional; therefore, the whole word is configurable).

11. Referring to claim 7, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1. Trimberger has not taught that a plurality of the fixed operators of the first data execution path is arranged to perform a plurality of fixed operations in independent lanes according to single instruction multiple data principles. However, Official Notice is taken that SIMD and the related advantages are well known and accepted in the art. Specifically, SIMD allows each execution unit to perform the same instruction on different data in the same cycle, thereby increasing data level parallelism. Higher parallelism will potentially result in higher throughput as more operations can occur at once. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger such that a plurality of the fixed operators of the first data execution path (Fig.2, component 100) is arranged to perform a plurality of fixed operations in independent lanes according to single instruction multiple data principles.

12. Referring to claim 8, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1. Trimberger in view of Haynes and Lodi has not taught that a plurality of the configurable operators of the second data execution path is arranged to perform multiple operations in different lanes according to single instruction multiple data principles. However, Official Notice is taken that SIMD and the related advantages are well known and accepted in the art. Specifically, SIMD allows each execution unit to perform the same

instruction on different data in the same cycle, thereby increasing data level parallelism. Higher parallelism will potentially result in higher throughput as more operations can occur at once. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger in view of Haynes and Lodi such that a plurality of the configurable operators of the second data execution path (Trimberger, Fig.2, component 120) is arranged to perform multiple operations in different lanes according to single instruction multiple data principles.

13. Referring to claim 9, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations performed (Trimberger: column 8, lines 5-17).

14. Referring to claim 10, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 9, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations performed from a field of an instruction defining a configurable data processing operation (Trimberger: column 7, lines 62-67; column 8, lines 1-17).

15. Referring to claim 11, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information comprising information controlling connectivity of the configurable operators (Trimberger: column 8, lines 35-37).

16. Referring to claim 12, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 9, comprising a control map associated with configurable operators

of the second data execution path, said control map being operable to receive at least one configuration bit from a configurable data processing instruction and to provide configuration information to the configurable operators responsive thereto (Trimberger: column 7, lines 62-67; column 8, lines 1-17).

17. Referring to claim 13, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 12, wherein said configuration information controls interconnectivity between two or more of said configurable operators (Trimberger: column 8, lines 35-37).

18. Referring to claim 14, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive either configuration information determining the nature of an operation to be performed or configuration information controlling interconnectivity from a source other than a configurable data processing instruction (Trimberger: column 8, lines 5-17; Figure 2; items 101, 102 and 123).

19. Referring to claim 15, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, wherein at least one configurable operator of the second data execution path is capable of executing data processing instructions with an execution depth greater than two computations before returning results to a results store (Trimberger: column 3, lines 10-27) (It is inherent that these complex functions will take at least two cycles).

20. Referring to claim 16, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising a switch mechanism for receiving data processing

operands from a configurable data processing instruction and switching them as appropriate for supply to one or more of said configurable operators (Trimberger: column 7, lines 45-50).

21. Referring to claim 17, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising a switch mechanism for receiving results from one or more of said configurable operators and switching the results as appropriate for supply to one or more of a result store and feed back loop (Trimberger: column 8, lines 51-59).

22. Referring to claim 18, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising a plurality of control maps for mapping configuration bits received from configurable data processing instructions to configuration information for supply to configurable operators of the second data execution path (Trimberger: column 3, lines 66-67; column 4, lines 1-10).

23. Referring to claim 19, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising a switch mechanism for receiving configuration information from a control map and switching it as appropriate for supply to configurable operators of the second data execution path (Trimberger: column 8, lines 5-17).

24. Referring to claim 20, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising configurable operators selected from one or more of: multiply accumulate operators; arithmetic operators; state operators; and cross-lane permuters (Trimberger: column 3, lines 10-27).

25. Referring to claim 21, Trimberger in view of Haynes and Lodi has taught a computer processor according to claim 1, comprising operators and an instruction set capable of performing one or more operations selected from: Fast Fourier Transforms; Inverse Fast Fourier

Transforms; Viterbi encoding/decoding; Turbo encoding/decoding; and Finite Impulse Response calculations; and any other Correlations or Convolutions (Trimberger: column 3, lines 10-27) (polynomial evaluation is used in FFT and IFFT).

26. Referring to claim 22, Trimberger has taught a method of operating a computer processor having control and data processing capabilities, said computer processor comprising:

a) a decode unit for decoding instructions (Fig.2, component 112).

b) a dedicated control processing facility comprising a control execution path having its own control register file (Fig.2, component 103, for instance) and an execution unit (Fig.2, component 100). Note that at least these two components may be combined and called a dedicated control processing facility.

c) a dedicated data processing facility (see Fig.2, and note that the dedicated data processing facility is interpreted to include at least components 100, 103, 120, and 131, where at least components 100 and 103 form the dedicated control processing facility as described above) having its own data register file (Fig.2, at least 130), the data processing facility comprising:

c1) a first data execution path including fixed operators (Fig.2, component 100).

c2) a second data execution path including at least configurable operators (Fig.2, component 120) and a controller (controllers are inherently present in processors), the method comprising:

- decoding a plurality of instructions to detect whether at least one data processing instruction, of said plurality of instructions, defines a fixed data processing instruction or a configurable data processing instruction (Trimberger: column 7, lines 45-50).

- causing the computer processor to supply said at least one data processing instruction to said first data execution path for processing when a fixed data processing instruction is detected and to said second data execution path for processing when a configurable data processing instruction is detected; and outputting results produced by said first data execution path when a fixed data processing instruction is detected and outputting results produced by said data execution path when a configurable processing instruction is detected (Trimberger: Fig.2 and column 7, lines 45-50).

d) Trimberger has not taught that the dedicated control processing facility also include a branch unit and a load/store unit. However, the examiner asserts that such units are very well known in the art and are advantageous for providing basic functionality. Branch units are clearly advantageous because they allow for execution of branch instructions. These are at least useful so that loops may be implemented. Loops allow for repeated execution of a block of code without writing the code repetitively within the program. Hence, code size may be decreased. Load and stores, on the other hand, allow for communication data to/from the register file and memory, thereby expanding the usable memory space. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger such that the dedicated control processing facility includes a branch unit and load/store unit.

c) Trimberger has also not taught said configurable operators pre-configured into a plurality of hardwired operator classes. However, both Haynes and Lodi have taught that FPGAs may be designed to include dedicated circuitry pre-configured into a plurality of hardwired operator classes. That is, Haynes has taught dedicated multiplier blocks, which may be programmably

interconnected to create larger multipliers. Similarly, Lodi has taught dedicated carry chains, which may be connected to form adders, for instance. See page 133 and section 3.1. Essentially, instead of a fully reprogrammable FPGA, as taught by Trimberger, Haynes and Lodia have taught programmable devices, such as FPGAs, that would include configurable operators pre-configured into hardwired multiplier and carry chain classes. The examiner asserts that it is well known in the art for FPGAs, such as the Xilinx Virtex, to include dedicated multipliers and carry chains. Such a configuration, with a programmable portion, and a dedicated portion, allows a programmer to achieve balance between programmability and speed for different applications. One of ordinary skill in the art would have recognized that the hardwired operators of Haynes and Lodi could be implemented in the FPGA of Trimberger. Such a modification would allow Trimberger to achieve both programmability and speed in cases where dedicated circuitry is faster than programmable circuitry. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger's gate array to include configurable operators pre-configured into a plurality of hardwired operator classes, as taught by Haynes and Lodi.

f) Trimberger, as modified, has further taught configuring the connectivity of said configurable operators in accordance with configuration information provided in an opcode portion of said configurable data processing instruction. See column 3, lines 31-33, and note that Trimberger would still select the connectivity of the operator classes via program instruction opcode.

Response to Arguments

27. Applicant's arguments filed on July 14, 2009, have been fully considered but they are not persuasive.

28. Applicant argues the novelty/rejection of at least claim 1 on pages 9-11 of the remarks, in substance that:

> "Trimberger does not disclose...a dedicated control processing facility comprising a control execution path having its own control register file, a branch unit, an execution unit, and a load/store unit."

29. These arguments are not found persuasive for the following reasons:

a) The examiner asserts that Trimberger, as modified, has taught such a concept. Specifically, claimed elements such as "dedicated control processing facility" and "dedicated data processing facility" are merely names. Hence, any one or more components may be combined in Fig.2 of Trimberger to realize such facilities. And, the control facility may include any of the well known components claimed by applicant. See the rejections above.

Conclusion

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

DeHon et al., U.S. Patent No. 6,052,773, has taught DPGA-coupled microprocessors in which both fixed and configurable data paths exist in parallel.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183